Design Considerations for High Data-Rate Pre-Amplifiers for Use in a Disk-Drive

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***Abstract*—In an effort to achieve higher data-rates in disk-drives, it has been proposed that moving the preamp closer to the head will improve writer performance. This paper will show that the opposite is true: moving the writer closer to the head degrades write current rise-time and overshoot. Although settling time is improved by moving the preamp closer to the head, impedance-matching techniques are sufficient to address this. Ironically, reader considerations may motivate Chip-On-Suspension (COS), but only for MR sensors that are either very high or very low impedance. This paper will detail the noise peaking that results from an impedance-mismatched reader input network. Both reader and writer performances can be improved by using novel architectures and by optimizing their respective interconnects.**

***Index Terms*—Bandwidth, disc-drive, disk-drive, head, impedance-matching, input-network, interconnect, MR, noise, preamp, reader, response, rise-time, writer.**

I. Writer Design Requirements

THERE are two independent design requirements that must be achieved for a high-frequency writer. First, a specified rise-time must be achievable for a given head load and interconnect. Second, the pattern dependant distortion must be maintained below a specified threshold. The requirements for the two goals are simply defined. For minimum rise-time, maximum voltage must be delivered across the head. One way to eliminate pattern dependent distortion is to ensure that every node of the system is at steady-state prior to the subsequent transition. With write current precompensation and fast rise-times, acceptable pattern dependent distortion levels may be achieved without strictly meeting this condition. The problem with achieving steady state is a difficult one; in that the time required for achieving steady state is the 1T-cell time. For example, if a writer is being designed for 1 Gbit/sec operation, the 1 T-cell time using a typical 16/17 code is 941 picoseconds. Not all of this 941 picoseconds is available for the purpose of allowing the nodes to settle and reach steady state. Because the natural response of the interconnect/head system is long compared with a 1 T-cell time, the preamp must drive the system with voltages that greatly exceed the steady state solution in order to achieve write current levels within the 1 T-cell time limit. Therefore, during the first portion of the write-current waveform, called the rise-time or transient portion, the system is not being driven toward steady state. Only the remaining time of the 1 T-cell can be used to achieve steady state. Again, since the natural time constant of the interconnect/head is long compared with the 1 T-cell, the writer must terminate the rise-time portion of the waveform at a point when the head is very near to steady state. This is writer design in a nutshell. Apply maximum voltage during the rise-time portion of the waveform, and then bring the system to steady-state before the next transition.

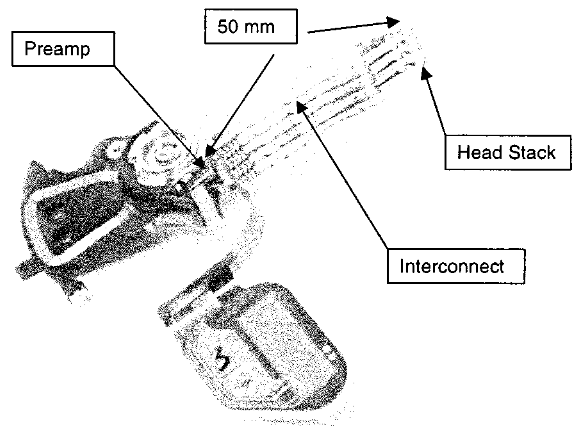

Fig. 1. E-block assembly of today's disk-drive.

II. Writer System Definition

The writer system consisting of a preamp, interconnect, and a read/write head is shown in Fig. 1. The head is located at the end of a suspension and is electrically connected to the preamp via approximately fifty millimeters of interconnect. The differential impedance (R_{TL}) of the interconnect is usually between 50 and 120 Ohms. The propagation time (τ_{TL}) for the interconnect is roughly 250 picoseconds.

This paper identifies the system parameters that enable the preamp designer to optimize the electronic response of the write-head. Here we will use the following typical write conditions:

$$\begin{aligned} V_{AVAIL} &= 8 \text{ Volts} \\ I_W &= 50 \text{ mA} \\ R_{TL} &= 50 \text{ Ohms} \\ \tau_{TL} &= 250 \text{ p sec.} \end{aligned} \tag{1}$$

A simple head model will be used for the writer analyzes, although the results are generally applicable to more complicated models such as the Klaassen head model [1]. Fig. 2 depicts

Manuscript received July 6, 2000.
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Publisher Item Identifier S 0018-9464(01)02267-1.

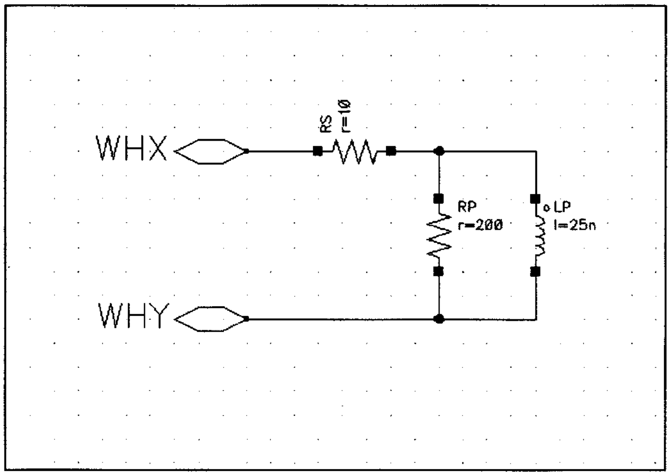

Fig. 2. Simple write head model.

this single energy-storage element model with typical elemental values given below:

$$\begin{aligned} L &= 25 \text{ nH} \\ R_P &= 200 \text{ Ohms} \\ R_S &= 10 \text{ Ohms}. \end{aligned} \tag{2}$$

III. Response of Single Energy-Storage Element Model with No Interconnect

The writer system equations will now be solved using the single energy-storage element write-head and no interconnect. This system simulates a preamp located immediately adjacent to a write head, and approximates a chip-on-suspension (COS) solution. The differential equation for the current in the inductive write element as a function of voltage applied by the preamp is given by:

$$V_{APP} = R_S I_L + L\left(1 + \frac{R_S}{R_P}\right)\frac{\partial I_L}{\partial t}. \tag{3}$$

The boundary conditions that will be used for this differential equation are those of an applied step function. Here, the applied voltage for times less than zero will be that voltage that creates a steady-state write current of $-I_W$. For times greater than or equal to zero, the applied voltage will be the supply limited voltage available to the preamp. The resulting boundary conditions are:

$$\begin{aligned} I_L(t \leq 0) &= -I_W \\ I_L(t \to \infty) &= \frac{V_{AVAIL}}{R_S}. \end{aligned} \tag{4}$$

The solution to this equation is given by:

$$I_L = -(I_W + I_0)\exp\left(\frac{-t}{\tau}\right) + I_0. \tag{5}$$

Here, the constants I_0 and τ are given by:

$$\begin{aligned} I_0 &= \frac{V_{AVAIL}}{R_S} \\ \tau &= \frac{L}{R_S}\left(\frac{R_S + R_P}{R_P}\right). \end{aligned} \tag{6}$$

IV. Response of Single Energy-Storage Element Model with Interconnect

The single energy-storage element write head model with an interconnect will now be evaluated. This system is representative of conventionally located preamps. The differential equation for the current in the inductive write element as a function of the voltage applied by the preamp is given by:

$$2V_{APP} = (R_S + R_{TL})I_L + L\left(1 + \frac{R_s + R_{TL}}{R_P}\right)\frac{\partial I_L}{\partial t}. \tag{7}$$

This differential equation is the same as that of a voltage source (having a source impedance of R_{TL}) driving the head. This voltage source delivers twice the voltage than that delivered by the source for the system without interconnect. This is how a transmission line system behaves for the first two delay times of the transmission line. This can be verified by evaluating the open head response and the short circuit response of this source. For an open head, the source delivers twice the applied voltage ($2V_{APP}$) for the first two delay time constants due to the reflection of the incoming signal. For the short circuit response, the current sourced is equal to twice the applied voltage divided by the differential impedance of the transmission line ($2V_{APP}/R_{TL}$) due to the negatively reflected wave.

The boundary conditions that will be used for this differential equation are again those of an applied step function. This time, however, the maximum current that can be delivered to the inductor is limited by the transmission line

$$\begin{aligned} I_L(t \leq 0) &= -I_W \\ I_L(t \to \infty) &= \frac{2V_{AVAIL} + 2I_W R_S}{R_S + R_{TL}} - I_W. \end{aligned} \tag{8}$$

The write current equation of this simple modeled is now given by:

$$I_L = -I_0 \exp\left(\frac{-t}{\tau}\right) + I_0 - I_W. \tag{9}$$

Here, the constants I_0 and τ are given by:

$$\begin{aligned} I_0 &= \frac{2(V_{AVAIL} + I_W R_S)}{R_S + R_{TL}} \\ \tau &= \frac{L}{(R_S + R_{TL})}\left(\frac{R_S + R_P + R_{TL}}{R_P}\right). \end{aligned} \tag{10}$$

Fig. 3 shows the natural response for both systems.

V. Analysis of Writer Located Near Write Head

When a writer is located near the write head, rise-time degradation occurs (in general) and interconnect related pattern dependency disappears. To demonstrate this, the solution to this system, given by (5) and (6), needs to be analyzed. If one solves (5) for the zero to 100% rise-time (the time until $I_l = I_W$), one finds:

$$t_{0\to 100\%} = \tau \ln\left(\frac{I_0 + I_W}{I_0 - I_W}\right). \tag{11}$$

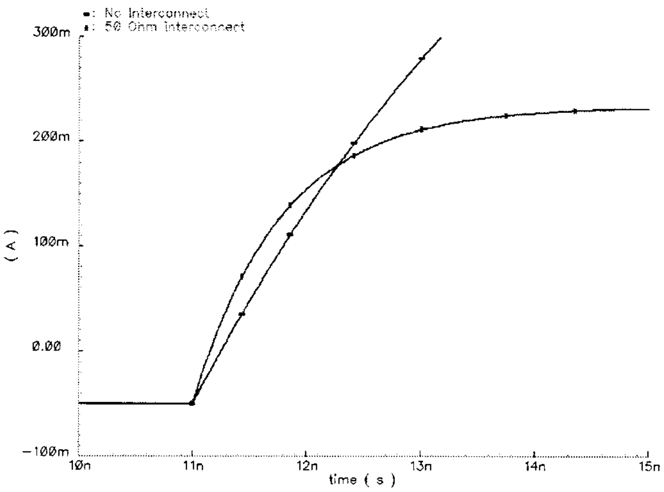

Fig. 3. Step response of simple head model with and without interconnect. Note that the system with interconnect exhibits faster initial rise-time.

Using our standard parameters for the write head and supply voltage, the $0 \rightarrow 100\%$ rise-time is equal to:

$$t_{0\rightarrow 100\%} = 329 \text{ p sec.} \tag{12}$$

By examining (11), one can see that there are two ways of decreasing the rise-time. First, one can reduce τ. Second, one can increase I_0. The head parameters determine τ completely, making τ a fixed function of the head. Substituting the solution for τ and I_0 given in (6) into (11) and approximating using truncated Taylor series results in:

$$t_{0\rightarrow 100\%} \approx L\left(\frac{R_S + R_P}{R_P}\right)\left(\frac{2I_W}{V_{AVAIL}}\right). \tag{13}$$

Thus the only parameter available to the system designer to reduce rise-time is the available voltage.

VI. Analysis of Writer with Interconnect between Head and Writer

When a writer is located far from the write head, with an interconnect between the two, rise-time is improved (in general) and interconnect related pattern dependency becomes an issue. The solution to this system is given by (9) and (10). Solving (9) for $0 \rightarrow 100\%$ rise-time results in:

$$t_{0\rightarrow 100\%} = \tau \ln\left(\frac{I_0}{I_0 - 2I_W}\right). \tag{14}$$

Using our standard parameters for the write head, supply voltage, and transmission line, the $0 \rightarrow 100\%$ rise-time is equal to:

$$t_{0\rightarrow 100\%} = 236 \text{ p sec.} \tag{15}$$

This improvement in rise-time is due to the "excess" voltage that the head sees due to the reflection of the write current wave at the write head. Because the rise-time of the writer system with interconnect is less than the writer solution without interconnect, a chip on suspension solution generally has a slower rise-time than a writer solution where the preamp is removed from the write head via an interconnect.

In this case, the two methods of decreasing rise-time must again be explored. In this case, the head parameters do not determine τ completely. The differential impedance of the interconnect affects τ and I_0. Substituting the solution for I_0 and τ given in (10) into (14) and approximating using truncated Taylor series results in:

$$t_{0\rightarrow 100\%} \approx L\left(\frac{R_S + R_P + R_{TL}}{R_P}\right)\left(\frac{I_W}{V_{AVAIL} + I_W R_S}\right). \tag{16}$$

In this case, reducing the differential impedance of the interconnect reduces the rise-time as does increasing the supply voltage. This improved rise-time comes at the expense of increased power. As the differential impedance of the interconnect is reduced, more current is delivered to it at a given applied voltage. Much of this current is reflected by the head and must be removed from the interconnect by the preamp termination. As the transmission line impedance approaches zero, the rise-time for the system with the interconnect is one-half that of the system without interconnect.

VII. Pattern Dependency and System Natural Time Constants

Reducing pattern dependent distortion to an acceptable level is a very difficult task of the preamp designer. Pattern dependent distortion has many sources. An improperly terminated transmission line between the channel and preamp will result in distortion of the write data at the input of the preamplifier. The large transient supply currents of the preamp during write mode causes the power supply to sag at the beginning of a write burst, which in turn affects the write data integrity. These large power supply transients also distort the input signal. This type of signal distortion falls into the classification of power supply rejection issues. Every circuit node in the preamp must be properly designed such that it reaches steady state prior to a subsequent transition. Finally, the transmission line and write head must reach steady state prior to a write current transition or the preamp must be impedance-matched to this transmission line. This interconnect system between the preamp and the write-head has traditionally been the largest contributor to pattern dependent distortion.

There are at least four methods of reducing electronic pattern dependent distortion to acceptable levels. First, one can allow the system to decay to steady-state naturally. Typical natural time constants for the preamp/write-head system, given by (6) and (10) are too long for today's data rates. Second, the system can be overdriven to decrease the time it takes to drive the system to the desired state. This technique is routinely employed by preamp designers. This method decreases the time that it takes the head to reach a targeted write current, however, it does not address pattern dependency. This technique must be combined with one of the following two techniques to eliminate electronic pattern dependency. Third, the preamp write-driver can be designed with an output impedance that matches the transmission line impedance. This coupled with overdriving the system is one solution to achieving steady-state within the 1-T cell time allotment without incurring pattern

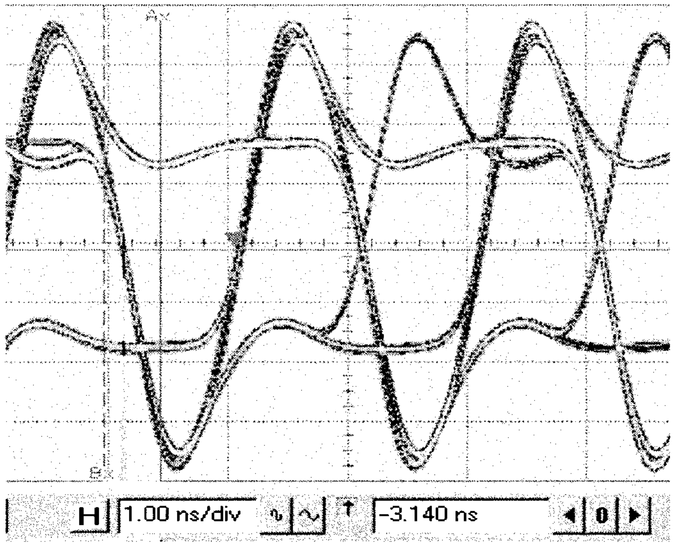

Fig. 4. Eye pattern of pseudo random data generated by an advanced impedance-matched writer into a simple head load. The peak current is 90 mA and the steady-state current is 40 mA.

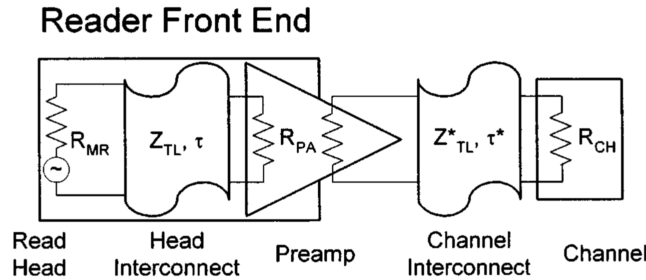

Fig. 5. Schematic showing reader front end.

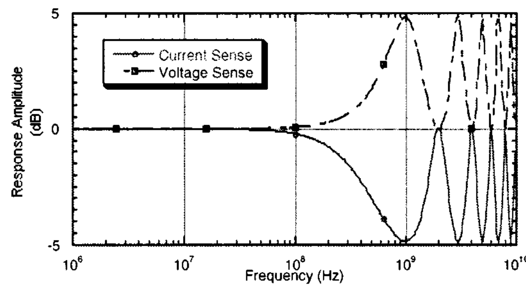

Fig. 6. Gain-Bandwidth plot for voltage-sense ($R_{PA} = 1000$) and current-sense ($R_{PA} = 10$) readers.

dependent distortion. Fig. 4 shows an eye pattern diagram for a preamp that uses this technique. Finally, moving the chip to the suspension combined with overdriving the head allows for reduced pattern dependent distortion.

VIII. Reader Technology

In today's 3.5 inch hard disk-drive, the front end consists of three components: a preamp, a spin valve read head, and an electrical interconnect that is approximately 50 mm long. The front end can be modeled as a transmission line with a source (MR head) and a load (preamp) attached to the end. Today's typical spin valve MR transducer has a nominal resistance ($R_{\rm MR}$) between 30 and 80 ohms. The differential impedance of the input network interconnect (R_{TL}) is usually between 50 and 120 ohms, and the differential input-resistance (R_{PA}) of the preamp is either low (less than 25 ohms) for a current-sense reader or high (greater than 200 ohms) for a voltage-sense reader. The propagation time (τ_{TL}) for the input network interconnect is roughly 250 picoseconds. The input network can degrade the signal response and noise figure of the read data path. For example, an input network whose preamp is impedance-matched to the interconnect has a significantly higher noise figure than that system in which the MR transducer is impedance-matched to the interconnect, even though both systems have frequency independent response characteristics. The remainder of this paper will detail the response and noise relations of the input network parameters.

IX. Effects of Interconnect and MR Resistance on Response

The input system or input network, which includes the MR transducer, the interconnect between the preamp and this sensor, and the preamp, is the single most sensitive system in the entire read-path. Here, the signal that the sensor generates is quite small (typically about 1 mV for today's production GMR transducers). Any noise produced here or coupled into this system will be amplified by the full gain that is used for signal amplification. Since this system is typically not impedance-matched, the response to the signal is not constant over frequency. Fig. 5 shows a schematic of the input network. Using transmission line analyzes such as those given by Johnson *et al.* [2], the signal transfer from MR transducer to preamp input is described by the following transfer function:

$$\begin{aligned} A_V &\equiv \frac{V_{PA}}{V_{\rm MR}} \\ &= \frac{R_{PA}Z_{TL}}{Z_{TL}(R_{PA}+R_{\rm MR})\cos\omega\tau + j(R_{PA}R_{\rm MR}+Z_{TL}^2)\sin\omega\tau}. \end{aligned} \tag{17}$$

Note that the gain (A_V) is a periodic function of frequency (ω). Note that the gain periodicity is solely determined by the interconnect propagation time and is independent of R_{PA}. In other words, the periodicity for a current-sense preamp is the same as that of a voltage-sense preamp.

Notice that the magnitude of the gain variation is equal for the two sense-schemes if the input-impedances of the two schemes are equivalently mismatched from the interconnect. For example, if the interconnect differential impedance is 100 ohms, a 1000 ohm voltage-sense preamp and a 10 ohm current-sense preamp have the same magnitude of gain variation. The voltage-sense response will show peaking, and the current-sense response will show attenuation. Fig. 6 shows the response plots of this input network for both voltage-sense and current-sense preamps that have equivalent transmission line mismatches.

X. Duality of Voltage-Sense and Current-Sense

Because both current-sense and voltage-sense architectures have the same periodicity and gain magnitude ratios, they are duals of one another. Two networks are said to be duals of one another if their responses are equal. Here, the two networks do not have equal responses, but the magnitude variation of their responses are equal as is the periodicity of the response variation. The term duality will be used here in a liberal fashion for lack of a better term. This duality occurs for a current-sense voltage-sense preamp pair in the specific case when their input-impedances are equivalently mismatched from the differential impedance of the interconnect. This results in reflection coefficients whose magnitudes are equal but whose signs are opposite. This gain ratio is due to reflections that are constructive or destructive. The magnitude of the peaking is roughly proportional to the product of the two reflection coefficients of the input network (K_{MR}) for small reflection coefficient products. Here K_{MR} is the reflection coefficient at the MR transducer end of the interconnect and K_{PA} is the reflection coefficient at the preamp. For an interconnect of differential characteristic impedance Z terminated in a resistance R, the reflection coefficient K at the termination is given as:

$$K = \frac{R - Z}{R + Z}. \tag{18}$$

For poorly matched systems ($R \gg Z$ or $R \ll Z$),

$$K \approx \pm 1. \tag{19}$$

Typically, voltage-sense and current-sense preamps present input-impedances that are poorly matched to the interconnect. In these cases,

$$K_{\mathrm{MR}} K_{PA} \approx \pm K_{\mathrm{MR}}. \tag{20}$$

In other words, the magnitude of the $K_{\mathrm{MR}}K_{PA}$ product is determined by the MR-interconnect mismatch and not by the preamp-interconnect mismatch. The sign of the $K_{\mathrm{MR}}K_{PA}$ product is determined by the preamp-interconnect mismatch or the sense scheme (typically $+$ for voltage-sense and $-$ for current-sense). This means that even for voltage-sense and current-sense preamps whose input-impedances are not equivalently mismatched from the interconnect differential impedance, they are still very nearly duals of each other.

XI. Noise Implications of Impedance Mismatch for Voltage-Sense and Current-Sense

The noise of a preamp can be decomposed into two components: a voltage-noise component and a current-noise component. Because the input network is impedance-mismatched, input referring these two noise-components results in frequency dependencies. Here, it will be shown that the two components have frequency responses that are opposite of one another. In other words, one noise component has a frequency response that peaks at resonance, while the other is attenuated at resonance. To solve for the input referred equivalent noise as a function of frequency, one needs to find the input network's impedance as a function of frequency. The equivalent impedance (Z_{EQ}) of the input network as seen from the preamp is given by:

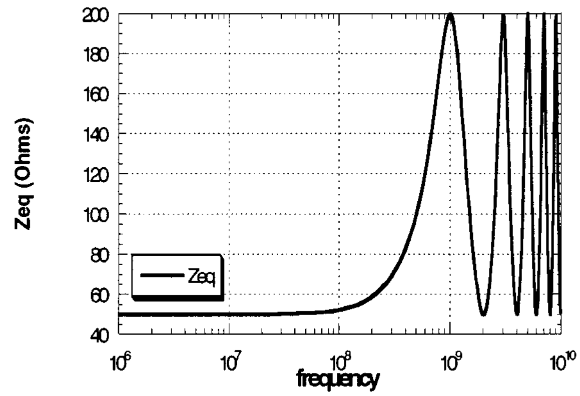

Fig. 7. Equivalent impedance seen from the preamp input looking toward the magnetic read head.

$$Z_{EQ} = Z_{TL}\,\frac{R_{\mathrm{MR}}\cos\omega\tau + jZ_{TL}\sin\omega\tau}{Z_{TL}\cos\omega\tau + jR_{\mathrm{MR}}\sin\omega\tau}. \tag{21}$$

Fig. 7 shows the plot of Z_{EQ} vs. frequency using typical values for the input network parameters. Note that the equivalent impedance peaking is greater than the gain peaking given in (17).

If one applies a current-noise source across the inputs of the preamp and evaluates the input-referred voltage-noise associated with this source, one obtains:

$$V_I^{\mathrm{input}-referred} = I_N^{preamp}\,\frac{R_{PA}Z_{EQ}}{R_{PA}+Z_{EQ}}\,\frac{1}{A_V}. \tag{22}$$

If one solves (22) using (17) and (21) the input-referred voltage-noise of the preamp's equivalent current-noise becomes:

$$V_I^{\mathrm{input}-referred} = I_N^{preamp}(R_{\mathrm{MR}}\cos\omega\tau + jZ_{TL}\sin\omega\tau). \tag{23}$$

If one now applies a voltage-noise source in series with the input of the preamp and evaluates the input-referred voltage-noise associated with this source, one obtains:

$$V_V^{\mathrm{input}-referred} = \frac{V_N^{preamp}}{A_V}. \tag{24}$$

If one now applies (17) and (21) to (24), the input-referred voltage-noise associated with the preamp's equivalent voltage-noise becomes:

$$V_V^{\mathrm{input}-referred} = \frac{V_N^{preamp}}{R_{PA}Z_{TL}}\,[Z_{TL}(R_{PA}+R_{\mathrm{MR}})\cos\omega\tau + j(R_{PA}R_{\mathrm{MR}}+Z_{TL}^2)\sin\omega\tau]. \tag{25}$$

Note that as one noise component increases, the other decreases. Because the two noise components are mostly uncorrelated, the two components add as the square root of the sum of squares. Even though one noise component is reduced at resonance, the total system noise is typically increased at resonance because of the lack of correlation. This noise peaking is often the dominant source of high frequency noise.

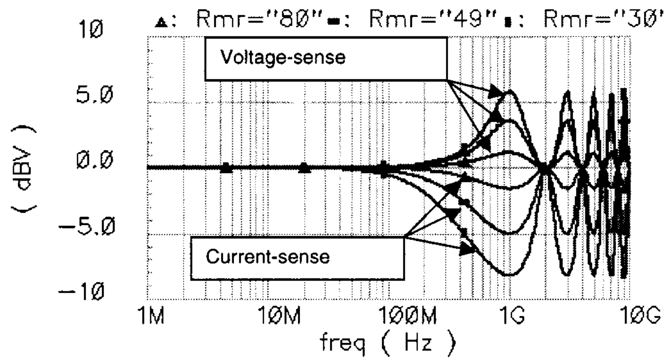

Fig. 8. Gain-Bandwidth for "today's" typical input network: $Z_{TL} = 100$ Ohms.

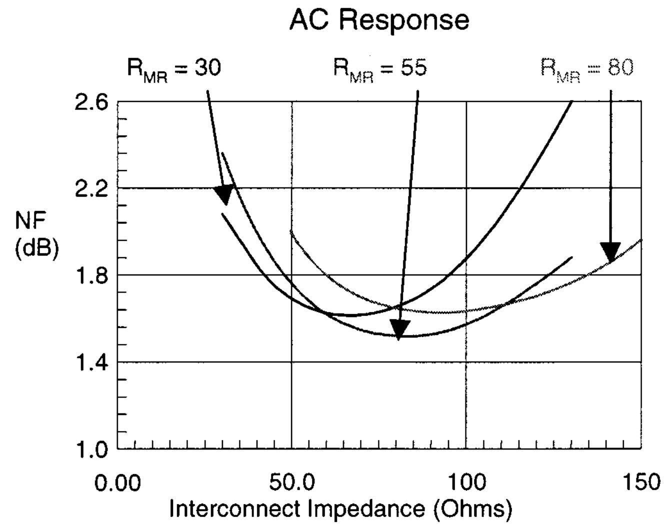

Fig. 9. Weighted integrated noise figure versus Z_{TL} for voltage-sense preamp.

Also noteworthy is that this noise peaking is a function of the impedance mismatch of the MR element and the transmission line. Designing a preamp with an input-impedance that matches the transmission line results in a flat signal response, but does not address the noise peaking. If the MR sensor is of an impedance that is outside of the practical values for the differential impedance of a transmission line, COS readers would reduce the system noise. Putting the reader closer to the head increases the resonant frequency of the input network, and thus pushes the noise peaking to frequencies (hopefully) outside of the reader pass-band.

XII. Consequences of MR Resistance Range

The specification for the range for the MR resistance is typically 30–80 ohms. Having such a large resistance range results in a large distribution of gain and noise responses (see Fig. 8). To optimize the worst-case response of the system, the differential-impedance of the transmission-line should be set to the geometric mean of the MR resistance range (49 ohms). The preamp frequency response is limited, however, by the high and/or low value of MR resistance. If the resistance range of the sensor were smaller, the frequency of operation would be correspondingly greater.

The noise of the system is also a function of the mismatch between the MR resistance and the transmission line differential impedance. Fig. 9 shows the weighted integrated noise figure of a preamp as a function of transmission line differential impedance. One way of optimizing the interconnect is to choose the value at which the high and low MR resistance noise responses cross. This value of interconnect differential impedance is generally quite near the geometric mean of the high and low MR resistances.

XIII. Summary

The need for input network parameter consideration is a new necessity for the preamp designer. Until reader bandwidth requirements became a large fraction of the input network resonant frequency ($1/4\tau$ or 1 GHz typically), the preceding high frequency issues were unimportant. Now that the bandwidths are high relative to the input network resonant frequency, the input network parameters have significant effect on the system performance. The following simplified statements summarize this paper.

- Conventionally located preamps have faster writer rise-times in general than preamps located on the suspension.
- Pattern dependent distortion can be minimized by either using impedance-matching techniques or moving the preamp closer to the head.
- Voltage-sense and current-sense reader architectures are duals. Neither architecture is inherently favorable for high bandwidth application.
- For optimal noise performance, the transmission line differential impedance should be set to the geometric mean of the high and low limits of the MR resistance range. This is also an optimal solution for the systems' bandwidth and group delay.
- Limiting the range of the MR resistance allows for higher bandwidth and improved noise performance.
- For MR sensors with impedances that are outside the range of practical interconnect-impedances, moving the reader to the suspension will likely be required to suppress the noise peaking of the impedance-mismatched system.

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